REMARKS

In the non-final Office Action of February 22, 2008, the Examiner: (1) rejected claims 1-4, 6-10, and 18-26 as allegedly obvious over Eggleston (U.S. Patent No. 6,906,961) in view of Wei (U.S. Patent No. 6,683,817) and Ito (U.S. PGPub 2004/0221098); (2) rejected claims 12-16 as allegedly obvious over Eggleston and Kikuchi (U.S. Patent No. 6,594,792); (3) rejected claims 5 and 11 as allegedly obvious over Eggleston, Kikuchi, Ito and Acton (6,883,131); and (4) rejected claim 17 as allegedly obvious over Eggleston, Kikuchi and Acton.

With this response, Applicant amends claims 1, 6, 12 and 18. Applicant believes that the pending claims are allowable over the art of record and respectfully request reconsideration.

I. ART BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly obvious over Eggleston, Wei and Ito. Applicant amends claim 1 to define over Ito's teaching of storing data read from the memory into shift registers to calculate check bits.

Ito is directed to a semiconductor integrated device. (Ito Title). Ito teaches an ECC-CODEC that produces check bits for error correction/detection with reference to data in the memory, and stores the check bits in a pre-determined region of the memory. (Ito Abstract). When the ECC-CODEC is operated as a coder the data read from the memory is supplied to feedback shift registers to calculate check bits based on the data read from the memory. (Ito Paragraph [0143]). After the check bits have been calculated check bits are then sent through a switch to be written to a write buffer. (Ito Paragraph [0144]). Thus, Ito appears to teach loading data read from the memory into feedback shift registers that are used to perform the logical operation to calculate check bits; but Ito does not teach storing ECC in a plurality of registers while transferring the data block.

Claim 1, by contrast, specifically recites "computing an ECC for said data block while transferring the data block; and selectively storing the ECC in a plurality of registers using a switching mechanism, the storing while transferring the data block." Applicant submits that Eggleston, Wei and Ito fail to teach or fairly suggest such a method. In particular, Ito appears to teach shift registers to calculate parity bits and a

switch to write the parity bits to a write buffer, but Ito is silent as to a switching mechanism that stores ECC in plurality of registers while transferring data. Thus, even if the teachings of Eggleston and Wei are precisely as the Office Action suggests (which the Applicant does not admit), Eggleston, Wei and Ito still fail to teach or fairly suggest "computing an ECC for said data block while transferring the data block; and **selectively storing the ECC in a plurality of registers using a switching mechanism, the storing while transferring the data block**."

Based at least on the foregoing Applicant submits that claim 1 all claims which depend on claim 1 (claims 2-5) should be allowed.

B. Claim 6

Claim 6 stands rejected as allegedly obvious over Eggleston, Wei and Ito. Applicant amends claim 6 to define over Ito's teaching of storing data read from the memory into shift registers to calculate check bits.

Claim 6 specifically recites "said controller is configured to shift a data block between the flash memory and the controller while computing an ECC for said data block; and said system is configured to selectively store the ECC in a plurality of registers using the switch, while the controller shifts the data block." Applicant submits that Eggleston, Wei and Ito fail to teach or fairly suggest such a system. In particular, Ito appears to teach shift registers to calculate parity bits and a switch to write the parity bits to a write buffer, but Ito is silent as to a switching mechanism that stores ECC in plurality of registers while transferring data. Thus, even if the teachings of Eggleston and Wei are precisely as the Office Action suggests (which the Applicant does not admit), Eggleston, Wei and Ito still fail to teach or fairly suggest "said controller is configured to shift a data block between the flash memory and the controller while computing an ECC for said data block; and said system is configured to **selectively store the ECC in a plurality of registers using the switch, while the controller shifts the data block**."

Based at least on the foregoing Applicant submits that claim 6 all claims which depend on claim 6 (claims 7-11 and 24-26) should be allowed.

C. Claim 12

Claim 12 stands rejected as allegedly obvious over Eggleston and Kikuchi. Applicant amends claim 12 to define over Ito's teaching of storing data read from the memory into shift registers to calculate check bits.

Claim 12 specifically recites "a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block; and a means for selectively storing the ECC in a plurality of registers while shifting the data block." Applicant submits that Eggleston and Kikuchi fail to teach or fairly suggest such a system. In particular, Ito appears to teach shift registers to calculate parity bits and a switch to write the parity bits to a write buffer, but Ito is silent as to a switching mechanism that stores ECC in plurality of registers while transferring data. Thus, even if the teachings of Kikuchi are precisely as the Office Action suggests (which the Applicant does not admit), Eggleston and Kikuchi still fail to teach or fairly suggest "a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block; and **a means for selectively storing the ECC in a plurality of registers while shifting the data block**."

Based at least on the foregoing Applicant submits that claim 12 all claims which depend on claim 12 (claims 13-17) should be allowed.

D. Claim 18

Claim 18 stands rejected as allegedly obvious over Eggleston, Wei and Ito. Applicant amends claim 18 to define over Ito's teaching of storing data read from the memory into shift registers to calculate check bits.

Claim 18 specifically recites "an ECC engine configured to compute an ECC while transferring a data block between the ECC engine and memory; and a switching mechanism coupled to the ECC engine, the ECC engine configured to selectively store the ECC in a plurality of registers using the switching mechanism, while transferring the data block." Applicant submits that Eggleston, Wei and Ito fail to teach or fairly suggest such a system. In particular, Ito appears to teach shift registers to calculate parity bits and a switch to write the parity bits to a write buffer, but Ito is silent as to a switching mechanism that stores ECC in plurality of registers while transferring data. Thus, even if the teachings of Eggleston and Wei are precisely as the Office Action suggests (which the

Applicant does not admit), Eggleston, Wei and Ito still fail to teach or fairly suggest "an ECC engine configured to compute an ECC while transferring a data block between the ECC engine and memory; and a switching mechanism coupled to the ECC engine, **the ECC engine configured to selectively store the ECC in a plurality of registers using the switching mechanism, while transferring the data block**."

Based at least on the foregoing Applicant submits that claim 18 all claims which depend on claim 18 (claims 19-23) should be allowed.

CONCLUSION

In course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Incorporated Deposit Account No. 20-0668.

Respectfully submitted,

/Utpal D. Shah/

Utpal D. Shah
PTO Reg. No. 60,047
CONLEY ROSE, P.C.
(512) 610-3410 (Phone)
(512) 610-3456 (Fax)
AGENT FOR APPLICANTS